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PC INTERFACING : DIGITAL FILTER REALIZATION

Amin Zeki Sadik

University of Salahaddin

College of Engineering

Dept. of Electrical Engineering

ABSTRACT

As PCs architecture is continuing its migration to embedded systems ,it has , increasingly, been involved in real-time operation as controllers. The price-performance ratio of embedded versions of PCs is very attractive . The reducing learning time resulting from using a familiar architecture also tends to lower development cost . This opens the door for wide range of applications. An excellent signal processing application that can introduce this approach is the realization of digital filter.

Digital filters have remarkable advantage over their analog counterparts; especially ,in low cut-off frequency responses .

A very low cut-off frequency digital filter has been designed and implemented by using the hardware resources of the PC .Various PC hardware facilities has been reviewed and efficiently used to carry out this research .

The application program is developed and written using 'C' language .

1. INTRODUCTION:

Today's PC architecture is continuing its migration to embedded systems .There are many reasons for this migration –as well as some problems this trend has met along the way [1].But cost still tops the list of forces causing a desktop machine's conversion to an embedded system.

The price-performance ratio of embedded PCs is very attractive .The reducing learning time resulting from using a familiar architecture also tends to lower development cost. Additional savings can be derived from the low cost of high-quality tools available in the PC world [2]. The PC open architecture related with the dramatic progress in the modern processors ,both in speed and performance (for example ,a processors throughput of about 1600 Mips has been released) , has made the implementation of high-speed real-time applications possible and desirable .

This research explores this approach and shows how various PC hardware resources can be utilized efficiently in specific application (the digital filter) and also discuses the bottlenecks of software and hardware that suffers from .

An excellent signal processing application that can introduce this approach is the realization of digital filter.

The most common meaning of the filter in the electronic context is as a type of circuit that separates signals at certain frequencies or band of frequencies from an input spectrum .However, these filters (analog type) ,usually constructed from resistor , amplifiers,capacitors ,and inductors seem far from the field of digital systems.

Digital filters have certain advantages over their analog counterparts ,specifically, insensitivity to change component values due to temperature or aging ,low cut-off frequency response ,flexibility and compatibility with digital transmission systems .

This later advantage is of increasing importance as digital communication systems come into wide use [3] .

Many of the applications of digital filters are associated with on-line equipment operating under real-time conditions, in-plant operating use in industrial environment .

2. DESIGN CONSIDERATIONS:

We are concerned here with the digital filter implementation and incorporation in digital system ,and for this reason ,we will need to know a little about their design limitations.

As with the process of A/D conversion ,one of these limitations is the representation of continuous process by a sampled digital series .

The range of frequencies that can be handled by a digital filter is limited by Nyquists' sampling criterion which states that the sampling frequency must be at least twice that of the bandwidth of the digital filter (to avoid aliasing).

Since digital filters are band-limited in this way and continuous analog filters are not, some form of approximation must appear when the digital equivalent of an analog filter is attempted .The most obvious measure of this approximation is the number of samples of the digital signal acted on by the digital algorithm.

Consider a digital series x_i , where i= 1,2,3,.....,n , performing a filtering action on this series means in practice that the individual numbers of the series are multiplied and combined in such a way as to produce a new modified series , y_i , which when converted into a continuous signal will have its frequency characteristics modified in the desired way.

We represent this mathematically by means of a linear difference equation from which the computing algorithm can be derived [4] :

$$y_i = \sum_{k=0}^{p} b_k \; y_{1-k} + \sum_{k=0}^{m} a_k \; x_{1-k} \quad \text{.....(1)}$$

p and m are positive integers representing the number of samples considered by the digital filter at any one time (its bandwidth) and a and b are a set of real constants defining the characteristic of the filter (low-pass,band-pass,frequency cut-off ,...).

The two basic types of digital filters are dependent on the values chosen for 'p' and 'm'. If we make p=0 and m equal to the order of the filter (a bandwidth factor which determines the fidelity with which the filter simulation approaches the continuous realization) then we have nonrecursive or finite impulse response (FIR) filter .

If we make m=0 and p equal to the filter order , then we have recursive or infinite impulse response (IIR) filter.

Digital filters can be realized either by hardware or by software simulation .A digital filter realized by using hardware method ,is fast and capable of high-speed real-time processing but is inflexible to change in frequency or filter characteristics and is usually expensive to implement .The software implemented digital filter was often carried out off-line using stored data and implementing the linear difference equation (1) is fairly direct fashion .

The filter characteristics can be readily altered by changing the values of p,m ,a, and b.

Before the advent of the microprocessor , the application of this method to real-time operation using dedicated digital computer was generally considered too expensive .The arrival of microprocessors has brought the possibility of programmable real-time digital filters [5] . When this development is associated with A/D converter under program control by the microprocessor ,we shall get a viable alternative to the analog filter which has proved to be extremely inflexible to design changes .

3. SINGLE-POLE DIGITAL LPF MODEL :

Recursive filter can be designed by either impulse-invariant method or bilinear Z-transform method .We are adopting ,here , the former one.

If the required digital filter has an impulse response as the prototype analog filter ,it is called an impulse-invariant digital filter , in which the analog filter is used to specify F(z) , the transfer function of the digital filter The simple analog filter is transformed into a digital filter in the following way[6] :

$$a/(s+a) \rightarrow a\,T/(1-e^{-aT}\,z^{-1}) \quad \ldots\ldots(2)$$

We want to design a discrete-time filter of recursive type with the frequency response of an analog single-section RC filter whose transfer function is given by :

$$H(s) = w_c/(w_c + s) \quad \ldots\ldots(3)$$

Where, $w_c = 1/RC$ defines the -3dB cutoff point .

Applying the transformation to equation no.(2) and (3) , we obtain the digital transfer function :

$$H(z) = w_c\,T/(1 - z^{-1}\,e^{-wc\,T}) \quad \ldots\ldots(4)$$

To obtain the difference equation , we convert from transform to sequence ,i.e. , taking the inverse z-transform to equation (3) . For a very low cut-off frequency of 0.1 Hz ,and sampling frequency of 1 Hz :

$$y(k) = 0.533\,y(k-1) + 0.628\,x(k) \quad \ldots\ldots(5)$$

Where, y(k) is the output (in time domain) in response to a step input .

4. REALIZATION AND RESULTS:

Both the hardware and the software will be introduced here :

(a) Hardware :

(i) IBM PC /AT bus :

AT style computers are based on the 80286 which has a 16-bit data bus , the 80386 which has a 32-bit data bus , or the 80386SX ,which is an 80386 having 16-bit data bus . 80486 is a 32-bit data bus ,which is the type used in this work (80486DX2).

These computers have a 16-bit expansion bus which actually consists of the original 8-bit bus plus an additional connector which has eight extra data bus lines , plus some further address and control lines . The expansion slots on the motherboard are ordinary 0.1 inch pitch female edge connector . The basic 8-bit slot has a 2 by 31 way connector ,with two rows numbered from A1 to A31 , and B1 to B31 .

The 16-bit expansion slot , which has been used here, additionally has a two-by-18 way female edge connector , with the two rows numbered from C1 to C18 , and D1 to D18 .Table(1) ,is a list of all the lines on the 8 and 16 bit expansion buses .

The IBM-compatible PC has a system timer which can be used to do software timing or time intervals during sampling action .The timer , i8254, which runs at 1.9318 MHz should theoretically be able to time intervals of 0.838095 μsec at very high precision .

However , there are a number of inherent limitations when using this system timer. The problems are : (1) interference from the system memory refreshment and (2) the 8254 timer is controlled by software which takes up a considerable amount of execution time .

These drawbacks can be evaluated , and we can work out the maximum errors attributed to each one of them[7] .

Also, the complete system hardware should use some high speed data transfer between the A/D converter and the PC memory . One way to carry out this is by using a direct memory access (DMA) facility . This method is adopted here .

The IBM-compatible PC/AT include in its standard hardware a DMA controller ,the i8237, which controls such operation .All it need is to properly program the controller to the: suitable mode , the number of transferred bytes and the address of PC memory into which these data to be placed .

The DMA cycle is initiated by the end-of-conversion pulse from the 12-bit A/D converter ,AD574A.

The application program ,see fig.(2), first initializes the PC timer (8254) to the required time interval which corresponds to the sampling period ,T, to control the action of real time digital filter operation.

It is clear that the maximum sampling rate (1/T) the digital filter can reach is limited by : (1) the time required by the A/DC to complete its conversion ,(2) plus the time required to complete the DMA transfer ,(3) plus the time required to complete the calculations of the mathematical model ,(4)

Slot No.	Function	Slot No.	Function
A1	-I/O CH CK	B1	GND
A2	D7	B2	RESET DRV
A3	D6	B3	+5V
A4	D5	B4	IRQ2
A5	D4	B5	-5V
A6	D3	B6	DRQ2
A7	D2	B7	-12V
A8	D1	B8	OWS
A9	D0	B9	+12V
A10	-I/O CH RDY	B10	GND
A11	AEN	B11	-MEMW
A12	A19	B12	-MEMR
A13	A18	B13	-IOW
A14	A17	B14	-IOR
A15	A16	B15	-DACK3
A16	A15	B16	DRQ3
A17	A14	B17	-DACK1
A18	A13	B18	DRQ1
A19	A12	B19	-REFRESH
A20	A11	B20	CLK
A21	A10	B21	IRQ7
A22	A9	B22	IRQ6
A23	A8	B23	IRQ5
A24	A7	B24	IRQ4
A25	A6	B25	IRQ3
A26	A5	B26	-DACK2
A27	A4	B27	T/C
A28	A3	B28	BALE
A29	A2	B29	+5V
A30	A1	B30	OSC
A31	A0	B31	GND
C1	BHE	D1	-MEM CS16
C2	LA23	D2	-I/O CS16
C3	LA22	D3	IRQ16
C4	LA21	D4	IRQ11
C5	LA20	D5	IRQ12
C6	LA19	D6	IRQ15
C7	LA18	D7	IRQ14
C8	LA17	D8	-DACK0
C9	-MEMR	D9	DRQ0
C10	-MEMW	D10	-DACK5
C11	D8	D11	DRQ5
C12	D9	D12	-DACK6
C13	D10	D13	DRQ6
C14	D11	D14	-DACK7
C15	D12	D15	DRQ7
C16	D13	D16	+5V
C17	D14	D17	-MASTER
C18	D15	D18	GND

'-' : Active-low signal.

Table(1),PC Bus Slot Numbers and Their functions.

and finally (if timing is critical) plus the time delays due to the unavoidable error sources resulted from the PC system ,such as, the refreshment overhead and delay caused by the hardware interrupt bus cycle .

(ii) Address decoder :

The first decision that has to be made when designing a PC card is just where in the input/output map it should be placed .Only 1024 (A_0 - A_9) possible I/O address available on a PC , and the lower 512 address are reserved for the computer internal hardware .Much of the upper block of 512 addresses are reserved for essential and standard expansion cards such as serial ports and display adapters . The full list of the PC I/O map allocation is shown in Table(2)[8] .

Although the I/O channel addresses range seems to be rather crowded , there are actually a few gaps that can be exploited. Also, the address range 300H-31FH is explicitly for prototyping cards, which would presumably embrace user add-ons .This gives some 32 addresses , which should be sufficient for most purposes .

Also the address decoder must process line AEN ,which is high during DMA cycles , and low during processor cycle .

IOR and IOW lines must also be considered to produce separate read and write outputs.

Although there are countless ways of decoding , I used (and I recommended the use) a single 74S138 3-to-8 line decoder to implement the address decoder .

(iii) IBM-PC and the 12-bit A/DC interface :

The AD574A successive approximation analog-to-digital converter interfaces to the IBM-PC bus as shown in the fig.(1) .

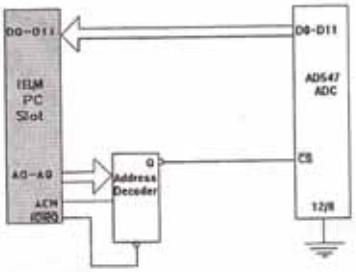

Fig.(1) . The hardware of the PC - ADC interfacing .

Designed to be port mapped , its address is decoded from the lines $A_0 - A_9$. The address must be gated with AEN to mask out internal DMA cycles using the same I/O space .Decoder's output (active low signal) is applied to CS to initiate the conversion .

Only 12 bits out of the 16-bit data bus are used for the input port , the upper nibble (D_{12} - D_{15}) is masked out by application program .

(b) Application program :

The application program has been developed using the Turbo-C 2.00 compiler .As will be seen later , I intended to use the

System:

Hex Address Range	Function
000-01F	DMA Controller #1
020-03F	Interrupt Controller #1
040-05F	8254 Timer
060-06F	Keyboard Interface
070-07F	Real Time Clock
080-09F	DMA Page Register
0A0-0BF	Interrupt Controller #2
0C0-0DF	DMA Controller #2
0F0	Clear Processor Busy
0F1	Reset Processor
0F8-0FF	Arithmetic Processor

I/O Channel:

Hex Address Range	Function
1F0-1F8	Fixed Disk
200-207	Game Port
210-217	Expansion Unit
220-24F	Reserved
278-27F	Parallel Port 2
2F0-2F7	Reserved
2F8-2FF	Serial Port 2
300-3F1	Prototype Card
320-32F	Fixed Disk
360-36F	Reserved
378-37F	Parallel port 1
380-38F	SDLC Bisynchronouos #2
3A0-3AF	Bisynchronouos #1
3B0-3BF	Monochrome Display/Print Adapter
3C0-3CF	Reserved
3D0-3DF	Color Graphics Adapter
3F0-3F7	Floppy Disk Controller
3F8-3FF	Serial Port #1

Table(2),System and I/O Map.

maximum power (or facilities) of the PC in order to cover a wide range of possible applications and , of course , for maximum flexibility in our present application .

The application program synchronizes the operation of the unipolar A/D converter , conditioned to process signals in the range of 0 – 10 V with a data capture and display routines. Fig.(2) , shows the flow chart of the program .

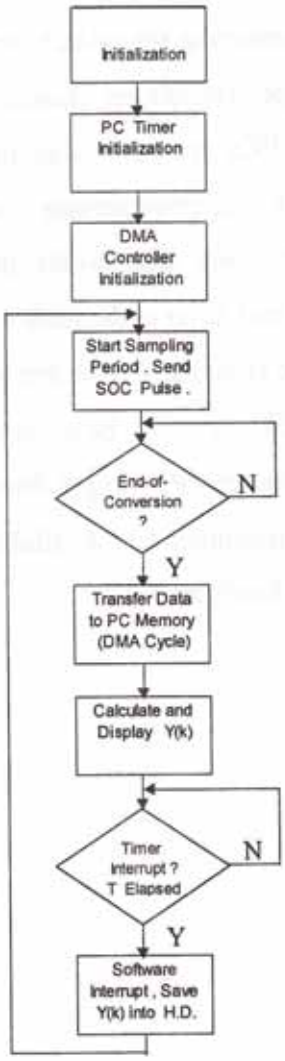

Fig.2: Flow Chart of the Application Program.

Polling techniques are excluded completely from the program , and instead , interrupts are used so as to allow another tasks ,if any , to be worked out .

For instance, after the sampling period has elapsed , the timer will initiate an interrupt , and an interrupt service routine will be executed to display and store the output response .

(c) The Results:

The output response of the digital filter is stored into the hard disk in real-time operation and displayed on the screen .However, this process of storing data into the hard disk is slow ,relatively ,and may be not practical in higher frequency cut-off filters .

If you want to take the advantage of this method and in the same time to eliminate the problem of slow operation of the H.D , you can use a ROM –disk card with suitable capacity and access time .

Figure no. (3) shows the response of the digital LPF ,with cut-off frequency of 0.1 Hz and sampling rate of 1 Hz, for unit-step input signal.

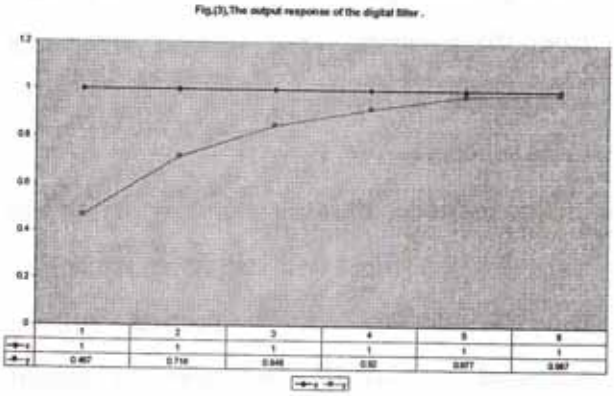

Fig. (3) The output response of the digital filter

5.CONCLUSION:

The PC architecture is continuing its migration to embedded systems. There are many reasons for this migration , as well as some problems this has met along the way . But cost still tops the list of forces causing desktop machines conversion to an embedded systems .

However, in now days it seems that the price-performance ratio of embeddable version of PCs is very attractive .Interfacing the PC has been achieved by direct connection to the internal PC/bus (16-bit) . Hardware resources , such as , interrupt controller , DMA controller , and system timer are used to carry out the digital filter . Also , their bottlenecks has been introduced and specified thoroughly .

This approach found great acceptance in applications requiring flexibility ,extensive facilities ,standardization and interactive capabilities .Industrial process control and complex measuring set-up in biomedical and laboratory applications are examples of such.

In fact, PCs are now ,due to the great advances in microprocessor speed and performance, used extensively in real-time applications and as an embedded system.

For these reasons , I intended to carry out the digital filter , may be as part of certain task, by using the PC to get the benefits of the standard resources and available on-shelf software and hardware.

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الارتباط بالحاسب الشخصي : تحقيق مرشح رقمي

أمين زكي صادق
جامعة صلاح الدين / كلية الهندسة
قسم الهندسة الكهربائية

الخلاصة

بسبب أستمرار تحول معمارية الحاسب الشخصي نحو الانظمة المطمورة , فأنها دخلت بشكل متزايد في عمليات السيطرة في الزمن-الحقيقي . ان نسبة الكلفة/الاداء للحاسبات الشخصية المطمورة أصبح جذابا جدا . كذلك فأن تقليل زمن التعلم في تلك الانظمة المطمورة , بسبب المعمارية المألوفة للحاسب الشخصي أدت أيضا الى تخفيض كلفة التطوير . كل هذا أدى الى فتح الباب أمام تطبيقات واسعة المدى .

ان تحقيق مرشح رقمي يعتبر تطبيقا ممتازا في مجال معالجة الاشارة و يمكنه ان يعرف بهذا المنحى . ان المرشح الرقمي يمتلك مزايا حسنة مهمة بالمقارنة مع المرشح التناظري , و خاصة في مدى الاستجابة الترددية الواطئة جدا .

لقد تم في هذا البحث تصميم و تنفيذ مرشح رقمي ذو تردد قطع واطئ بأستخدام موارد الكيان المادي المختلفة للحاسب الشخصي المتوافق مع IBM عن طريق الارتباط المباشر مع ناقل الاشارات .

تمت كتابة البرنامج التطبيقي بأستعمال لغة 'C'.

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بەکارهێنانی کۆمپیوتەر لەبنیادنانی فلتەری ژمێرەیی

امین زکی صادق
بەشی ئەندازیاری کارەبا
کۆلیژی ئەندازیاری
زانکۆی سەلاحەدین-هەولێر

کورتە

لەبەرئەوەی بینای کۆمپیوتەر بە بەردەوامی بەرەو سیستەمی یەکپارچەیی هەنگاو دەنێت، بۆیە بەکارهێنانی کۆمپیوتەر لەکۆنترۆڵکردنی دەسبەجێدا لەگەشە سەندنایە. ڕێژەی پارەی تێچوو بۆ جۆری کارکردنی ئەم جۆرە کۆمپیوتەرانە زۆر کەمە. ئەمەو لەگەڵ کەمبوونەوەی کاتی پێویست بۆ فێربوونی ئەم سیستەمە یەکپارچانە بۆتە هۆی کەمکردنەوەی پارەی گەشەپێدانی. هەموو ئەو هۆیانە بۆتە هۆی بەرفراوان بوونی بەکارهێنانی.

بەکردەوەکردنی فلتەرێکی ژمێرەیی بەکارهێنانێکی نایابی ئەم سیستەمانەیە لەچارەسەرکردنی سیگنالەکان. فلتەری ژمێرەیی لەفلتەری بڕی باشترە بەتایبەتی بۆ وەلامدانەوەی لە لەرەلەرە نزمەکاندا. دروستکردنی فلتەرێکی بڕی لەو لەرەلەرە نزمانە ئەگەر ئەستەمیش نەبێ ئەوا زۆر زەحمەتە.

لەم توێژینەوەیەدا، فلتەرێکی ژمێرەیی بە لەرەلەری بڕینێکی زۆر نزم نەخشەی بۆ کێشراوەو جێبەجێ کراوە لەرێگای کۆمپیوتەرێکی هاوجۆر لەگەڵ IBMدا. پڕۆگرامێکی کۆنترۆڵکردن بەزمانی C بۆ سیستەمەکە نووسراوەو ڕوێنراوە.